

Poster presentation

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Temporal spike pattern learning

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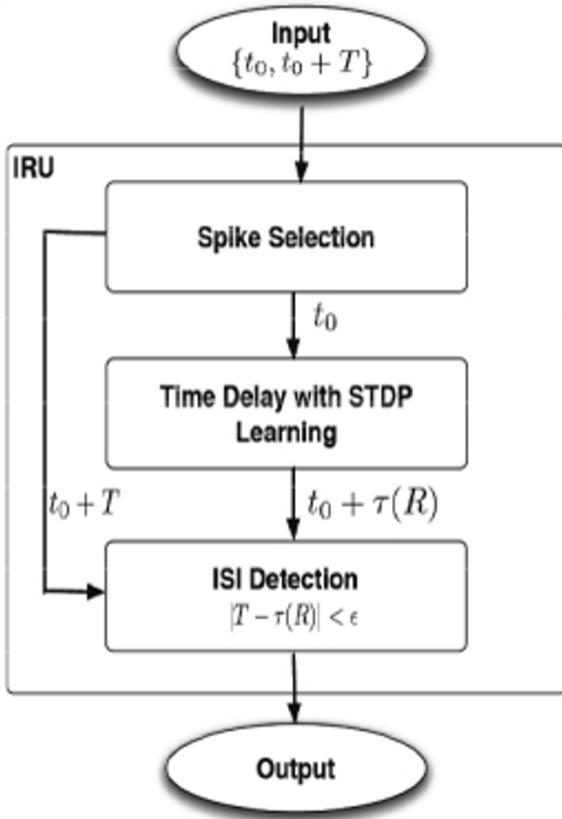
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Sensory systems pass information about an animal's environment to higher nervous system units through sequences of action potentials. When these action potentials have essentially equivalent waveforms, all information is contained in the interspike intervals (ISIs) of the spike sequence. The question then is, how do neural circuits recognize and read these ISI sequences? We address this issue of temporal sequence learning with a neuronal system utilizing spike timing dependent plasticity (STDP).

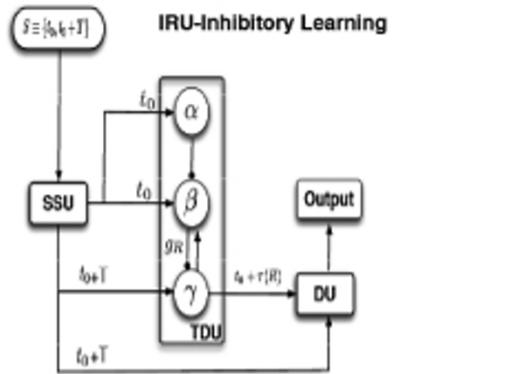
Motivated through recent work by [1] using spike timing dependent plasticity rules observed in inhibitory synapses, we present a very general architecture of neural circuitry that can perform the task of ISI recognition. The essential ingredients of this neural circuit, which we refer to as "interspike interval recognition unit" (IRU) are, (i) A spike selection unit, the function of which is to selectively distribute input spikes to downstream IRU circuitry, (ii) A time delay unit that can be tuned by STDP, (iii) A detection unit, which is the output of the IRU and a spike from which indicates successful ISI recognition by the IRU (Fig 1a). We present two distinct configurations for the time delay circuit within the IRU using excitatory and inhibitory synapses respectively to produce a delayed output spike at time $t_0 + t(R)$ in response to an input spike received at time t_0 (Fig 1b, c). R is the tunable parameter of the time delay circuit that controls the timing of the delayed output spike. We discuss the forms of STDP rules for excitatory and inhibitory synapses respectively, which allows for modulation of R for the IRU to perform its task of ISI recognition. We then present two architectures for

the IRU circuitry that can both learn the ISIs of a training sequence and then recognize the same ISI sequence when it is presented on the subsequent occasion.

a Interspike interval Learning Unit (IRU)



b IRU-Inhibitory Learning



c IRU-Excitatory Learning

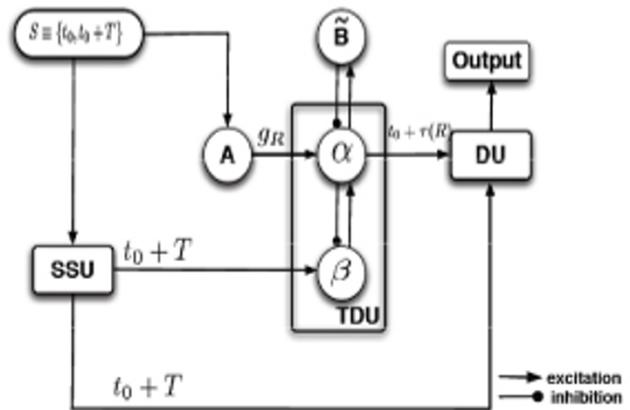


Figure 1

(a) Schematic diagram of the Interspike interval Recognition Unit (IRU). The IRU will respond with an output spike if it is tuned to detect the input interspike interval T . The key circuit elements of the IRU are, (1) a spike selection unit (SSU), whose function is to split the incoming spike train into sequence of individual spikes to be fed into the downstream IRU circuitry, (2) a time delay unit (TDU), which can produce a delayed spike output at time $t_0 + \tau(R)$ in response to input spike at time t_0 , tuned through either an excitatory or inhibitory spike timing dependent learning rule, (3) a detection unit (DU), which triggers a spike output if it receives coincident spike input through the TDU. (b) Schematic circuitry for the IRU constructed with a TDU that can be tuned through spike timing dependent plasticity of an inhibitory synapse (iSTDP). (c) Schematic diagram of the IRU constructed using a TDU that can be tuned through spike timing dependent plasticity of an excitatory synapse (eSTDP).

Acknowledgements

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References

1. Abarbanel HDI, Talathi SS: **Neural circuitry for recognizing interspike intervals.** *Phys Rev Lett* 2006, **96**:148104.

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